Characterization of Surface- and Buried-Channel Detection Transistors for CCD On-Chip Amplifiers

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Abstract

Low noise floating-diffusion amplifiers, made in double and single layer membrane poly-Si technology, are characterized including scaling rules for the 1/f noise, thermal noise, 3 dB bandwidth and conversion gain. A comparison is made between buried- and surface-channel detection node transistors for various channel widths, lengths, and bias currents. A new method for measuring the total detection node capacitance is used. The results are modeled using a noise model that includes shot noise from hot-electron effects.

Introduction

A new image-sensor technology for making very small pixels was developed and recently reported [1,2]. Using this technology for the on-chip amplifier poses two possible problems: the high resistance of the membrane poly-Si (thickness: 50 nm) and contacts to the membrane poly-Si above active silicon. For this reason new amplifiers were tried using only one or two layers of membrane poly-Si.

Fig. 1 shows a 3-stage source follower with M1, M2, and M3. An important characteristic of the new technology is that the surface-generated leakage current is very low. This lowers the 1/f noise generation in the detection transistor (M1). In the past, 1/f noise cross-over frequencies were as high as 10 MHz which made it nearly impossible to use surface-channel MOS transistors for detection. This paper shows that in this new technology the 1/f noise generation is almost the same for both surface-channel and buried-channel types. Therefore both transistors are candidates for future amplifiers. The imagers in which these amplifiers will be used have pixel frequencies above 5 MHz. The effect of the 1/f noise on the signal-to-noise ratio is negligible when its cross-over frequency with the thermal noise is well below the clocking frequency [3]. Fig. 2 shows typical noise spectral densities for an on-chip amplifier in which the first MOS transistor is of the surface- or buried-channel type. It shows that both surface and buried MOS transistors have very good and almost equal 1/f noise performance. Fig. 3 shows the cross-over frequency as a function of the gate area (WL) of the detection transistor. It demonstrates that this frequency has reached such a low level that the contribution to the signal-to-noise ratio after CDS is negligible for clocking speeds above 5 MHz. Thus, to optimize the noise of these amplifiers one has only to focus on the thermal noise.

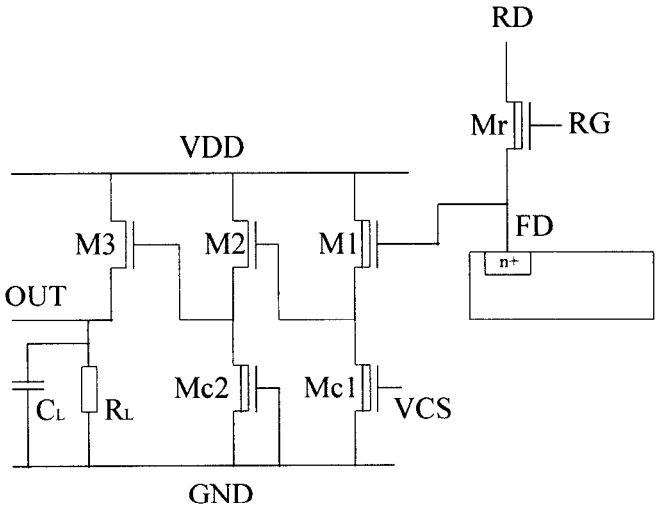

Fig. 1: Schematic view of the floating-diffusion amplifier. Transistor M1 can be of the surface- or buried-channel type.

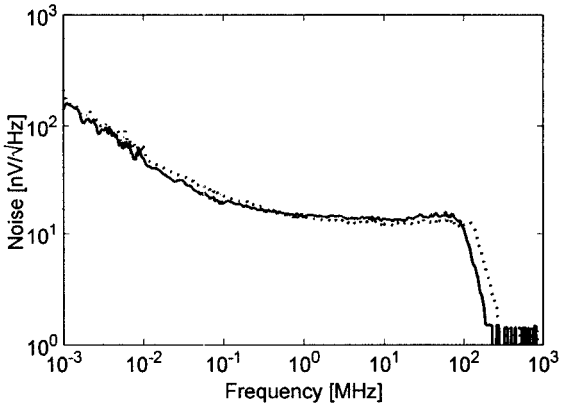

Fig. 2: Typical noise spectral densities for an amplifier in which the detection transistor (M1) is of the buried-channel (solid line) or surface-channel type (dotted line). Both detection transistors have the same size. The cross-over frequencies in the case of buried channel and surface channel are 94 kHz and 216 kHz, respectively.

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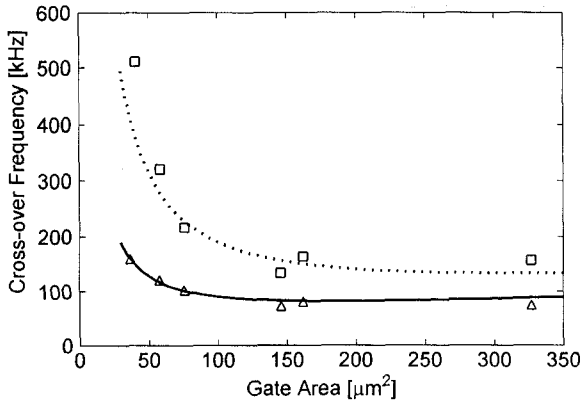

Fig.3: Cross-over frequency as a function of gate area of the detection transistor for buried-channel transistors (triangles) and surface-channel transistors (boxes). The markers are measurements and the curves are the predictions from the model.

Thermal Noise

The thermal noise of a MOS transistor is determined by its transconductance, the backbias effect, and shot noise caused by hot-electron effects. The noise ideality factor (α) [4,5,6], which is the product of the equivalent noise resistance (R_n) of a MOS transistor and its transconductance, is given by:

$$\alpha = R_n g_m = \frac{2}{3}\left(1 + \frac{g_b}{g_m}\right) + \frac{I}{g_m}\frac{\rho}{L} \qquad (1)$$

where g_m is the transconductance, g_b the transconductance of the backbias, I the bias current, L the channel length, and ρ a constant for the shot noise term. In the ideal case α is 2/3. For the surface channel the backbias effect is negligible. The buried channel is deeper below the surface, therefore creating a bigger backbias effect. Fig. 4 shows the measured α for surface- and buried-channel MOS transistors as a function of current densities. It shows clearly that even for moderate current densities hot-electron effects exist. The effect is less pronounced for the buried-channel transistor due to the use of retarded source and drain regions, which act as an LDD implant, and because the channel acts like a JFET. The model shows a good fit with the measurements.

Noise Electron Density

To determine the noise electron density (NED) [7] the total capacitance (C_t) at the detection node (FD) was measured in two steps. First, the responsivity (μV/e) at the output node and the gain from floating diffusion to output were measured, and from this the effective sense capacitance C_{in} was calculated (see Fig. 5). Second, the sensitivity improvement factor θ_n (= C_t/C_{in}) was measured using the gate of the current source (Mc1 in Fig. 1) as an injection point and measuring the gain from this gate to the output. Fig. 6 shows that with only one measurement the sensitivity improvement factor can be determined. This guarantees identical voltage settings for the reset FET (Mr) on- and off-state. The product of θ_n and C_{in} results in the total capacitance. Fig. 7 shows C_t as a function of W and L for both surface- and buried-channel transistors. From the slope and intercept of these lines it is possible to determine how the capacitances are distributed. The noise electron density (NED) is the product of the equivalent noise voltage at the input of the on-chip amplifier and C_t. In Fig. 8 it is shown as a function of W for both the surface- and buried-channel transistors. In these measurements VCS is set so that 60 μA bias current flows

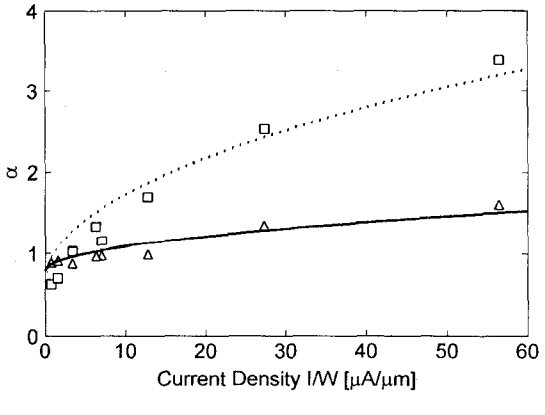

Fig. 4a: Noise ideality factor (α) as a function of current density (I/W) for buried-channel type (triangles) and surface-channel type (boxes) (for fixed L). The markers are measurements and the curves are the predictions from the model (eq. 1).

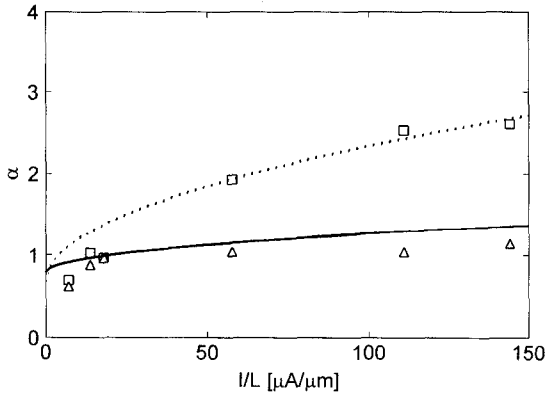

Fig. 4b: Noise ideality factor (α) as a function of I/L for buried-channel type (triangles) and surface-channel type (boxes).(for fixed W). The markers are measurements and the curves are the predictions from the model.

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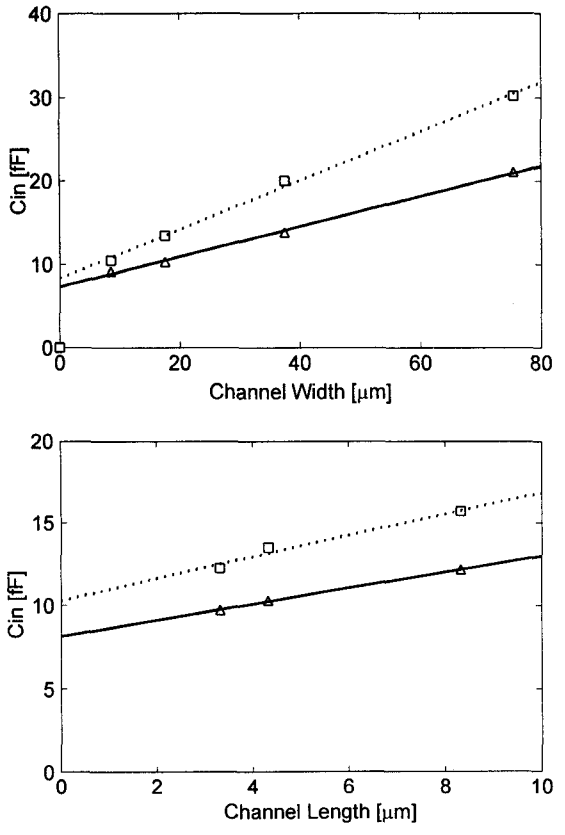

Fig. 5: Effective sense capacitance as a function of the channel width (for fixed L) and channel length (for fixed W) of the detection transistor in case the transistor is of the surface channel (boxes) or buried channel (triangles). The lines fit the measured data.

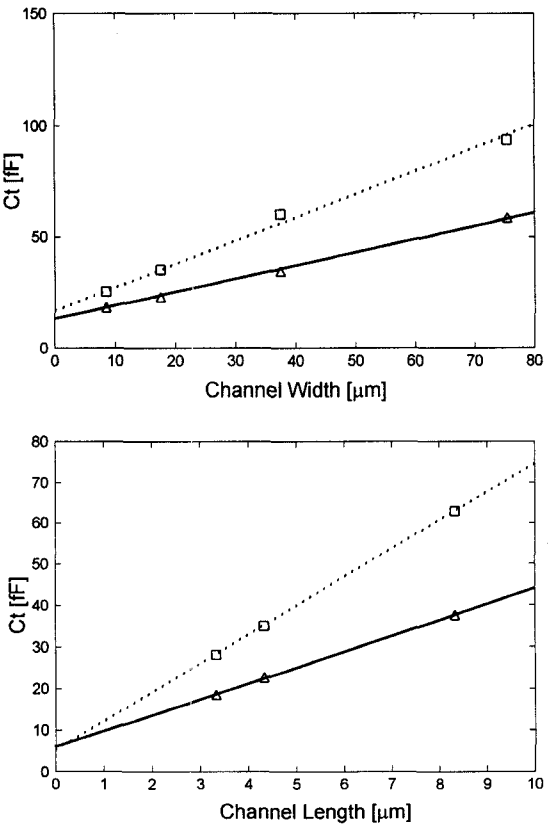

Fig. 7: Total capacitance as a function of the channel width (for fixed L) and channel length (for fixed W) of the detection transistor in case the transistor is of the surface channel (boxes) or buried channel (triangles). The lines fit the measured data.

through the first stage of the amplifier. One can see that the noise performance of both transistors is nearly the same, because the somewhat higher C_t of the surface transistor is compensated by the higher transconductance. From the NED model, which includes α and C_t, the optimal width for the surface transistor is found to be 9 μm and for the buried channel 13 μm. It shows a good fit with the measurements.

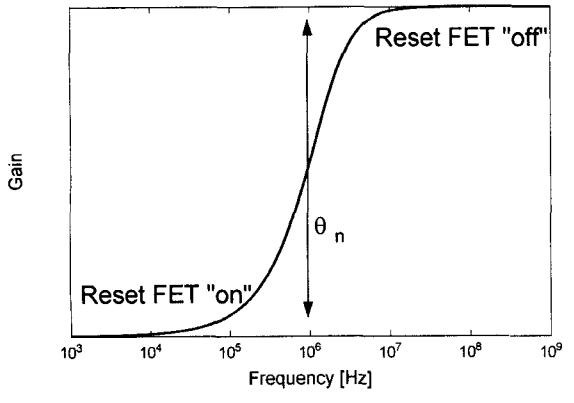

Fig. 6: Measurement of the sensor improvement factor (θ_n) for a typical device. VCS (see Fig. 1) is used as input while the reset gate (RG) potential is fixed.

Bandwidth

The bandwidth in the reset FET off-state determines the signal shape [7] and the possibility for reset noise suppression. A method has been developed to determine this bandwidth by using the dominant noise of the first source follower stage. Above the 1/f cross-over frequency this noise source is white and is therefore usable as an internal source for bandwidth measurements. Fig. 9 shows the 3dB bandwidth as a function of the channel width. The 3 dB bandwidth (F_{3dB}) is given by:

$$F_{3dB} = \frac{g_m}{2\pi\theta_n A_1 C_L} \qquad (2)$$

with g_m the transconductance of the first source follower, θ_n the sensitivity improvement factor, A_1 the DC-gain of the first source-follower stage, and C_L (Fig. 1) the load capacitance at

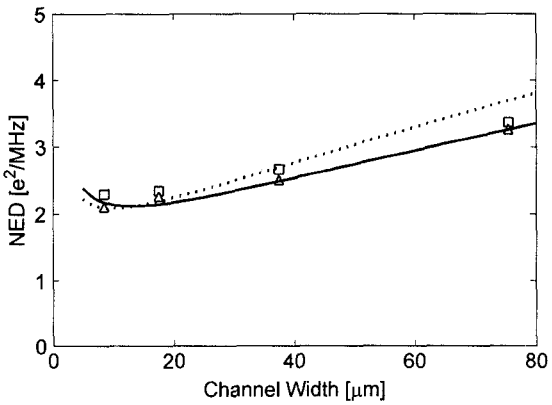

Fig. 8: NED versus the channel width for the surface channel (boxes) and buried channel (triangles) (for fixed L). The curves are the predictions from the model.

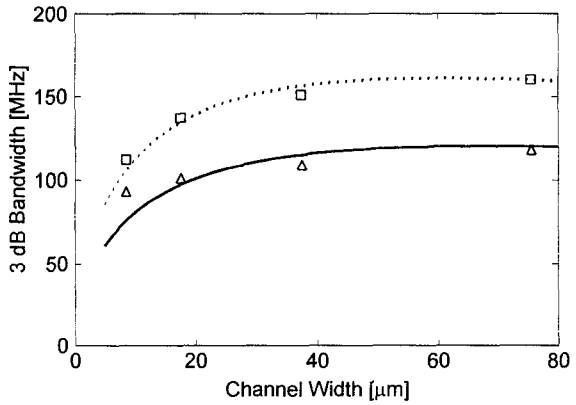

Fig. 9: 3dB bandwidth versus the channel width for the surface channel (boxes) and the buried channel (triangles). The lines correspond to the model.

the source of the first source follower. In the region of interest the bandwidth increases for larger channel width, just as the noise does.

Conclusion

On-chip amplifiers have been successfully made in single and double membrane poly-Si technology. Because of the lower sense capacitance, the buried-channel detection transistor has a higher conversion gain than the surface-channel transistor, while the transconductance of the surface transistor is higher than that of the buried-channel transistor. This compensates the higher total capacitance, and as a result the noise performance is nearly the same for both transistors. Although both types have a very high bandwidth it is shown that the choice between high bandwidth and low noise is a conflicting one.

Acknowledgement

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References

[1] Peek, H.L., *et al.*, An FT-CCD Imager with true 2.4 * 2.4 μm² Pixels in Double Membrane Poly-Si Technology, *IEDM Tech. Dig.*, 1996.

[2] Peek, H.L., *et al.*, Technology and Performance of VGA FT-Imagers with Double and Single Layer Membrane Poly-Si Gates, *IEEE Workshop on CCD's and Advanced Image Sensors,* June 5-7, 1997, Bruges, Belgium.

[3] Kansy, R.J., Responce of a Correlated Double Sampling Circuit to 1/f Noise, *IEEE J. Solid-State Circuits*, Vol. SC-15, no. 3, pp374-375, June 1980.

[4] Hynecek, J., Design and Performance of a Low-Noise Charge-Detection Amplifier for VPCCD Devices, *IEEE Trans. ED.*, Vol. ED-31, no.12, Dec. 1984.

[5] Klaassen. F.M., On the Influence of Hot-Carrier Effect on the Thermal Noise of Field-Effect Transistors, *IEEE Trans. ED.*, Vol. ED-17, no. 10, Oct. 1970.

[6] Kim. S.K. and A.van der Ziel, Hot Electron Effect in Buried Channel MOSFET's, *Solid state Electronics.*, Vol. 24, pp 425-428, October 1981.

[7] Centen. P.G, CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions, *IEEE Trans. ED.*, Vol. ED-38, no. 5, May 1991.