A 2/3-inch Low Noise HDTV FT CCD-Imager for 1080i180, 1080p90 and 720p120 Scanning at Constant Image Diagonal

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Abstract

A novel broadcast FT-imager is presented that supports the 1080i, 1080p and 720p HDTV scanning formats at constant image diagonal. For super slow motion applications in 1080i/p it scans in 180 interlaced fields/sec or 90 progressive frames/sec or 120 frames/second in 720p. The anti-alias filtering is in the charge domain, automatically adapted to the scanning format. The imager reaches a pixel rate of 223Mpixel/sec. The on-chip amplifier has a bandwidth >241MHz. At 112MHz it has a Noise Electron Density of NED=0.59 e2/MHz and after CDS, 8 electrons in 30MHz bandwidth.

Introduction

The imaging technology for HDTV at 2/3" in broadcast [1,2,3,4] is becoming mature. Present state of the art allows for SNR values of 54dB at scene illumination levels of 2000lux f/8-f/11 with 90% scene reflection at 3200K color temperature and 30MHz video bandwidth. These values are reached while scanning at 1920x1080i60 (HxV and interlaced 60 fields/second). The discussion about the introduction of 1920x1080p60 (HxV and progressive 60 frames/second) is surpassed by the need for even higher frame rates of 1920x1080i180, also known as 3x. These tripled frame rates are needed for slow-motion recordings and playback in sports applications [5]. Vertical scanning, 1080i versus 720p or 1080p, is still a controversial topic. Imagers are designed to scan dedicated in 1080i/p [1,2,4] or 720p [3]. Imagers supporting 1080p60 can be readout in 720p60 fashion using region of interest scanning, [2]. The penalty is a reduction of the image diagonal from 11mm down to 7.3mm, causing a substantial change in viewing angle.

Building on DALSA's technology that employs thin transparent membrane gate electrodes and tungsten strapping [6,7,8] a novel imager is designed that supports the 1080i, 1080p, 720p native scanning formats at constant image diagonal. In 1080i the CCD delivers 180 fields/second, in 1080p it delivers 90 frames/second and in 720p, 120 frame/second. The imager has on-chip anti-alias filtering, in the charge domain, adapted to the scanning format. The method is based on pixel wobble, similar to the concept used in previous PAL and NTSC imagers [7]. The imager reaches a pixel output rate of 223Mpixel/sec. The imager reported in [3] only supports up to 720p96 at 118Mpixel/sec.

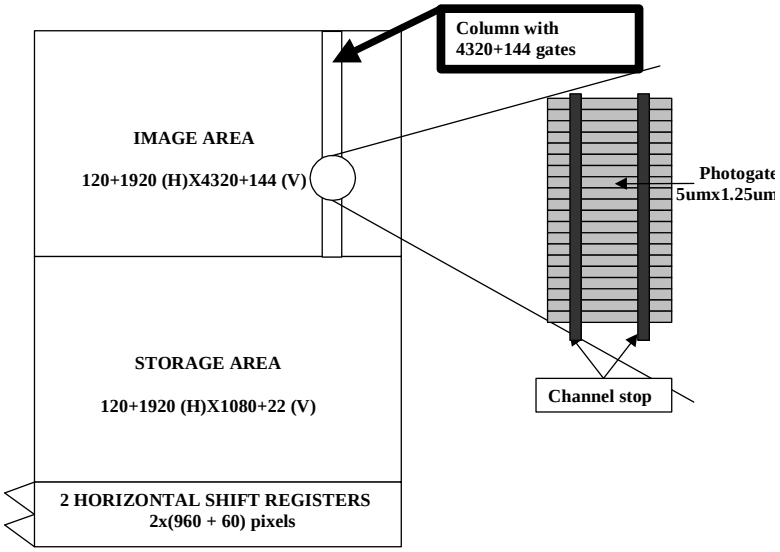

Figure 1a: *Schematic representation of the imager*

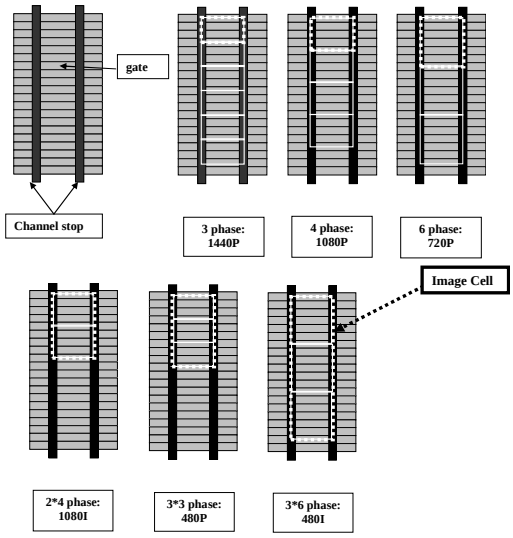

***Figure 1b**: various binning patterns.*

Constant Image Diagonal

Figure 1a shows a schematic representation of the imager. The image area has 4464 gates (V) and 2040 columns (H). Only 4320(V) x1920(H) is used to define the scanning format, the remaining positions are used for over scan and black reference pixels. The 4464 gates are connected through a 12-phase interconnect scheme. The height of one gate is 1.25um and the column width is 5um. Two horizontal registers are clocked at 111.375 MHz each and the vertical transport frequency is 9.28 MHz. The storage area has a fixed number of storage sites and includes the over scan- and black reference pixels, 2040(H) x1102(V), and has a 4-phase interconnect scheme.

During the horizontal line blanking a charge TV line, from the storage area, is distributed over the two readout registers with the 4-phases driven independently. During the active line time, when horizontal transport is at 2x111.375MHz, the horizontal register is driven in quasi-2 phase fashion Additional tungsten straps on the horizontal gates reduce series resistance, maximizing transport speed. The architecture of the two horizontal registers forces interleave between the pixels of top and bottom channel at the 2-outputs.

Figure 1b and Figure 2 denotes the possible vertical scanning formats in 16:9 aspect ratios. The first column describes the broadcast scanning formats. The choice for 4320 gates per column also enables the NTSC (480p, 480i) and PAL (576i) scanning standards and the cinemascope aspect ratio of 2.37:1 in 1080p.

The second column shows the number of gates to meet the required native scanning format and the third column shows how to achieve the scanning format given a 12-phase clocking and interconnect scheme, see also Figure 1b. Note that in 1080i the image area is scanned in 1080p and only in the horizontal registers the interlaced image is generated.

In the given scanning formats the active image width (H) is 1920x5um and the active image height (V) is 4320x1.25um. This results in an image diagonal of 11.0 mm for all scanning format as required for a 2/3" optical format.

16:9 scanning formats	**#GATES/Pixel**	**In 12-phase clocking schema**
1080p	4 (= 4320 / 1080)	4-phase clocking 1 pixel
720p	6 (= 4320 / 720)	6-phase clocking 1 pixel
1080i	8 (= 4320 / (1080/2))	4-phase clocking 2 sub-pixels
480p	9 (= 4320 / 480)	3-phase clocking 3 sub-pixels
576i	15 (= 4320 / (576/2))	3-phase clocking 5 sub-pixels
480i	18 (= 4320 / (480/2))	6-phase clocking 3 sub-pixels
1080p in 2.37:1 aspect ratio	3 (= 4320*(3/4) / 1080)	3-phase clocking 1 pixel

Figure 2: *Possible scanning formats at constant image diagonal, with 4320 vertical gates*

MOS Transistor oxide thickness

Signal-to-noise is an important parameter in broadcast applications. Especially at higher frame rates, with corresponding shorter exposure times fewer photon-generated electrons are collected and thus the sensitivity drops and lower readout noise levels are needed. A new on-chip amplifier was designed where special care was taken to reduce the floating diffusion and parasitic capacitances for enhanced conversion gain and reduced noise. The dimensions of the detection node source follower and output source follower are optimized and use is made of locally adapted oxide thickness of the MOS Transistors [9]

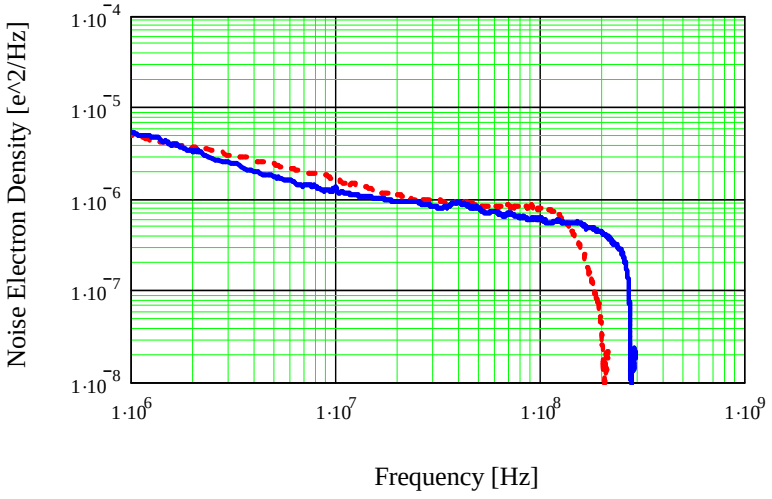

Figure 4: *Static noise measurement of the on-chip amplifier. Solid blue line is the new amplfier.*

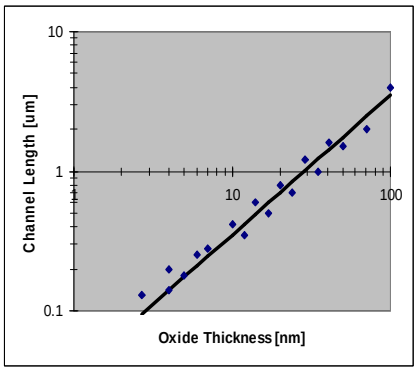

Figure 3: *Minimum channel length verus oxide thickness*

The classical parameters for noise optimization of the on-chip amplifier are the Width, the Length and the Bias current of the source follower in the detection node [10,11]. Noise optimization stops at the statement to make the channel length as small as possible. An additional degree of freedom for further optimization is found when the oxide thicknesses of the MOS transistors in the on-chip

amplifier are allowed to be chosen independently. Based on data from [12], a relation between minimum channel length versus oxide thickness can be plotted, **figure 3.** The straight line is given by $L_{\min} = 0.035 * d_{ox}$,.(L in µm and d in nm).

From [11] we know that the noise electron density (the noise power at a given frequency divided by the conversion gain of the on-chip amplifier) is written as $NED = \frac{4kT}{g_m} * \left(\frac{C_{tot}}{q} \right)^2$ and the noise bandwidth is $B_n \equiv \frac{g_m}{4 * C_{load}} \frac{C_{fd}}{C_{tot}}$. With g_m the transconductance of the source follower, C_{tot} the sum of all the capacitance connected to the floating diffusion and C_{fd} known as the detection node capacitance. The capacitance at the source, loading the source follower, is C_{load}. *Note that the bandwidth of the source follower stage is reduced during charge sensing this is due to the positive feedback from source to detection node*. Often Ctot≈Cfd is found for optimized detection nodes and hence the MOS transistor gate capacitance is determined. Using channel length proportional with oxide thickness, the channel width (W) of the source follower is determined too: *Cg = W.L.Cox only depend on W*

The first order approximation for the transconductance, using $I_{ds} = W * J_x$ with J_x=10A/m, is: $g_m = \sqrt{2 * \frac{W}{L} * \frac{\varepsilon}{d_{ox}} * u_n * I_{ds}} \approx \frac{W}{d_{ox}} \approx \frac{1}{d_{ox}}$. As discussed the gate capacitance of the source follower is determined for lowest noise and the width (W) is determined. This leaves only the oxide thickness as a parameter for control of the transconductance and hence noise (NED) and bandwidth (B_n). Halving oxide thickness doubles the bandwidth and reduces the noise with 3dB.

Figure 4 shows the measured noise spectrum (blue solid line) of the new 3-stage on-chip amplifier in comparison with the prior one (red dotted line). Parameter extraction revealed a 1/f corner frequency of 16MHz with an exponent of 0.83 and a 3dB bandwidth of 241MHz. This includes bandwidth limitation of the external instrumentation amplifier. The new amplifier has a NED=0.75e^2/MHz at 37MHz and at 112MHz, NED=0.59e^2/MHz. After CDS this results in 8e in 30MHz bandwidth.

In **Figure 5** the state-of-the-art amplifier noise performance is given using reference to the reset frequency [8]. Noise levels in the range of 4.6 to 2 electrons are reported [2,13,14] but only for CMOS imagers and only at a high gain setting of the column amplifiers, reducing saturation level at the same time, or with 4 channel readout [14]. In the past sub-electron noise levels where reported for CCDs but always for bandwidths less than 1MHz.

Type	**Ref**	**Reset Frequency**	**Ampl. Type**	**Conversion gain**	**Noise after CDS/ √Resetfrequency**
FF-CCD	ED1997 Burke	100 kHz	Source Follower	20 µV/e	6.3 e/√MHz
CMOS	AIS2003 Krymski	50 kHz	Source Follower +Gain	60 µV/e	6.3 e/√MHz
FF-CCD	AIS2005 Draijer	25 MHz	Source Follower	40 µV/e	2.8 e/√MHz
CMOS	ISSCC2005 Kozlowski	104 kHz	Source Follower +Gain	?µV/e	46 e/√MHz
CMOS	ISSCC2006 Yoshihara	156 kHz	Source Follower +Gain	40 µV/e	17.7 e/√MHz
CMOS	ISSCC2007 Takahashi	156 kHz	Source Follower +Gain	75 µV/e	11.6 e/√MHz
CMOS	ISSCC2007 Cho	625 kHz	Source Follower +Gain	101 µV/e	10.4 e/√MHz
FT-CCD	This paper	111MHz	Source Follower	18 µV/e	1.3 e/√MHz

Figure 5: *State-of-the-art amplifier noise performance*

In interpreting the noise levels one must also take into account that in CMOS imagers each column has its own CDS part. The readout time of a CMOS pixel is on a 1us time scale, while the CCD imager presented here outputs pixels on a 9ns time scale and hence the noise is generated in a much larger bandwidth.

Summary

The overall performance of the imager is summarized in figure 6. The scanning formats are 1920x1080i180, 1920x1080p90 and 1920x720p120. The noise after CDS is 8 electrons in 30MHz bandwidth, the saturation level is 680 electrons/µm^2 and a sensitivity of 820 electrons/lux/sec/ µm^2 in green is reached. These performance parameters are reached simultaneously and are noted per unit area because of the diversity of scanning formats with its different pixel area.

In conclusion, this is the first CCD HDTV imager reported supporting 1920x1080i180, 1920x1080p90 and 1920x720p120 at a constant image diagonal of 2/3-inch.Together with the simultaneous improvements in clock frequency, bandwidth, noise, saturation level and sensitivity the state of the art is advanced.

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Technology	Tungsten, thin transparent membrane Frame Transfer CCD		Number of horizontal registers	2
Chip Size	12.0(H) x 12.7(V) mm^2		Number of horizontal clock phases During fast horizontal transport	4 Quasi 2-phase operation
Aspect Ratio	16:9		Number of on-chip amplifiers	2
Storage number of clock phases	4		Measured bandwidth of on-chip amplifier	>241MHz
Storage number of columns x lines	2040(H) x 1102(V)		Conversion gain	18 µV /e
Image number of clock phases	12		Max frame rate, pixel rate	180 fld/sec, 223Mpixel/sec
Image number of columnsxgates	2040(H) x 4464(V)		Horizontal transport frequency	2x112MHz
Pixel size in 1920x1080p90	5.0 µm x 5.0 µm (HxV)		Vertical transport frequency	10MHz
Pixel size in 1920x1080i180	5.0 µm x 5.0 µm x 2 (HxV)		Noise Electron Density (NED) of the on-chip amplifier	0.75 e^2/MHz@37.125MHz 0.59 e^2/MHz@112MHz
Pixel size in 1920x720p120	5.0 µm x 7.5 µm (HxV)		Temporal Noise After CDS in 30MHz	8e or 2.1 e^2/MHz
Pixel size in 1920x1080p90 @ 2.37:1	5.0 µm x 3.75 µm (HxV)		Sensitivity in Green	820 electrons/lux/sec/μm^2
			Qmax	680 electrons/μm^2

Figure 6: *Performance and device summary*

References

[1] M. Morimoto et al;" A 2/3-inch 2 M-pixel IT-CCD image sensor with individual p-wells for separate V-CCD and H-CCD formation", ISSCC. Dig. of Tech. Papers., pp. 222 - 223, Feb. 1994

[2] L. Kozlowski et. al, "A Progressive 1920x1080 Imaging System-on-Chip for HDTV Cameras", ISSCC Dig. Tech. Papers, pp. 358 - 359, Feb. 2005.

[3] T. Honda et al, "Development of 2/3"-type 1-mega pixel Progressive Scan CCD for HDTV capable of high frame rate of 96fps". Proc. of the IEEE AIS workshop, pp.177 - 180, June , 2005

[4] P. Centen et al, A 2/3-inch CMOS Image Sensor for HDTV Applications with Multiple High-DR Modes and Flexible Scanning, ISSCC Dig. Tech. Papers, pp 512-513, Feb. 2007.

[5] T. Moelands et al, "A High Speed Sports Action Camera System", Dig. Of Tech. Papers IBC, pp. 86-92, Sept., 1998

[6] H. Peek," A Low Dark Current Double Membrane Poly-Si FT-technology for 2/3 Inch 6M Pixel CCD Imagers", Tech. Dig. IEDM, pp 871 – 874, Dec. 1999

[7] H.Stoldt et al, Invited, "CCD Imagers for Broadcast Applications". Tech. Dig. IEDM, pp. 899-902, Dec., 1996.

[8] J. Bosiers et al.," Technicall challenges and recent progress in CCD imagers", Nuclear Instruments and Methods in Physics Research, A 565, pp 148 - 156, May 2006.

[9] P. Centen private communications, 2005.

[10] J. Hynecek.; *Design and performance of a low-noise charge-detection amplifier for VPCCD devices*, Electron Devices, IEEE Transactions on, Volume 31, Issue 12, Dec 1984 Page(s):1713 - 1719

[11] P. Centen, *CCD on-chip amplifiers: noise performance versus MOS transistor dimensions*, Electron Devices, IEEE Transactions on, Volume 38, Issue 5, May 1991 Page(s):1206 - 1216

[12] P. Wong, *Technology and device scaling considerations for CMOS imagers*, Electron Devices, IEEE Transactions on, Volume 43, Issue 12, Dec 1996 Page(s):2131 – 2142

[13] A. Krymski et al. "A 2 e Noise 1.3Megapixel CMOS Sensor", Proc. of the IEEE AIS workshop, June 2003.

[14] H. Takahashi," A 1/2.7-inch Low-Noise CMOS Image Sensor for Full HD Camcorders", ISSCC Dig. Tech. Papers, pp:510 – 511, Feb 2007.